REMARKS

Claims 1-16 are pending in the application. Claims 1, 9 and 14 have been amended by the present amendment, and are fully supported by the specification as originally filed.

Claims 1, 9, and 14 were rejected under 35 USC 112, first paragraph, "as failing to comply with the written description requirement" by not including support for the limitation "temporarily linked to the supporting..." (Office Action, Page 2). Claims 1, 9, and 14 have been amended to remove the word "temporarily," and now recite "the substrate being linked to the supporting bars." Support for this language is provided in the specification (see, e.g., page 6, lines 4-5; page 7, lines 1-2; page 7, lines 21-22; and page 8, lines 16-17). Withdrawal of the rejection is respectfully requested.

Applicants' claimed invention is directed to a substrate strip including a frame having two supporting bars, and at least one substrate linked to the supporting bars by means of no more than two tie bars (i.e., less than the four tie bars disclosed in the prior art). The substrate, which does not include the tie bars, receives a semiconductor package formed on the substrate.

For example, as shown in FIG. 2A, substrate 110 is bordered by tie bars 131 and 132. As recited in claims 1, 9, and 14, the Applicants' claimed invention is restricted to one or two tie bars. Moreover, the substrate and semiconductor package are severed from the tie bars (i.e., cut along the dashed lines shown in FIG. 2A), such that the semiconductor package formed on the substrate is free of the tie bars.

The above-described substrate strip can provide significant benefits over the prior art. During a high-temperature step (such as molding, etc.) due to the reduced number of tie bars, the substrate experiencing thermal stresses can freely expand toward corners not having the tie bars, thereby preventing warpage and ensuring proper planarity of the substrate (see specification at page 6, lines 9-20). In contrast, in the prior art, the substrate is linked to supporting bars by four tie bars at four corners of the substrate, such that the thermal stresses concentrate toward the center of the substrate and thus produce warpage.

Claims 1-6, 9, 10, and 13 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,925,934 to Lim. Based on the statement on page 4 of the Office Action, it is assumed that claims 11 and 12 also were rejected over Lim. Claims 7 and 14-16 were rejected under 35 USC 103(a) as being unpatentable over Lim in view of U.S. Patent 5,847,446 to Park et al. (hereinafter "Park"). Claim 8 was rejected under 35 USC 103(a) as being unpatentable over "Lim and Park in view of admitted prior art." These rejections are respectfully traversed.

Lim and Park, whether taken alone or in combination, fail to teach or suggest a substrate strip having a substrate connected by only one or two tie bars to a frame so as to prevent warpage of the substrate. Moreover, Lim and Park do not teach or suggest that a semiconductor package formed on the substrate is free of the tie bars.

Lim, as shown in FIGS. 10A and 11, discloses the use of two tie bars 530, which are formed at opposite sides of a cavity 575 of a frame 570 to support and hold a chip 505 in the cavity 575 by attaching the chip 505 to the tie bars 530 via a die attach 540, so as to ensure stability of the chip 505 during handling and especially during the encapsulation process (see column 7, lines 21-26). The tie bars 530 are severed from the frame 570 and remain attached to the chip 505 in the fabricated package (see column 6, lines 23-24; FIG. 10A).

Therefore, in Lim, the tie bars 530 secure the chip 505 in position during an encapsulation process, but do not allow thermal expansion of the substrate and prevent package warpage, as taught in the Applicant's invention. Moreover, the tie bars 530 of Lim are encapsulated together with the chip and retained in the package; in contrast, the tie bars of the Applicants' claimed invention are cut and not contained in the semiconductor package.

Park cannot be combined with Lim to produce the Applicants' claimed invention, e.g., as recited in claim 14. Park discloses a chip attach pad 120 (see FIGS. 3 and 5) characterized by having a plurality of slots 124 formed in a perimeter region thereof, to allow a molding compound 160 to be contained within the slot 124 and adhered to the lower surface edges of the chip 110 so as to prevent delamination or crack formation. As shown in FIG. 5, four tie bars 122

are located at corner positions and joined to the chip attach pad 120. As stated in column 4, lines 23-26 (also cited in the Office Action), "[t]he package 200 ... may further comprise at least one tie-bar 122 which is joined to the chip attach pad 120. The tie-bar 122 provides the chip attach pad 120 with a mechanical stability."

Therefore, in Park, the tie-bar 122 is included in the package 200 for mechanically supporting the chip attach pad 120, whereas the Applicants' claimed invention requires that the "semiconductor package formed on the substrate is **free of the tie bar**" (claim 14).

For at least the above reasons, Lim or Park, whether each reference is taken alone or in combination with the prior art, do not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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